

D1  
--FIG. 2A shows a first TFT structure. In the first structure, an island-shaped polysilicon layer 204 is formed on a glass substrate 201, and a gate insulation film 206 is formed on the glass substrate 201 so as to cover the polysilicon layer 204. A gate electrode 208 is formed on the gate insulation film 206 so as to be just above a central portion of the island-shaped polysilicon layer 204.--

IN THE CLAIMS:

Please enter the following amended claims 1 and 22:

- D2  
Wnif  
Sub  
E1
1. (Four Times Amended) A method of manufacturing thin film transistors comprising the steps of:
- (a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;
    - (i) forming a gate insulating film on and across an intermediate region of each of the semiconductor layers, the gate insulating film having a thickness not larger than 50 nm, and exposing end regions of each of the semiconductor layers;
    - (ii) forming a gate electrode on the gate insulating film over each of said semiconductor layers, the gate electrode being retarded from edges of the gate insulating film, defining in each of the semiconductor layers a channel region below the gate electrode,

Sub  
E1  
Cont

and a pair of offset regions below the gate insulating film between the channel region and the end regions;

(b) implanting dopant into the offset regions in each of said semiconductor layers through the gate insulation film by ion implantation to form lightly doped regions; and

D2  
Unit

(c) implanting dopant into the end regions in each of said semiconductor layers directly to form heavily doped source/drain regions whose impurity concentration is higher than that of said lightly doped regions,

wherein said ion implanting steps (b) and (c) are so selected that hydrogen ions are also implanted into said lightly doped regions and said heavily doped source/drain regions, but not into said channel region under said gate electrode, and

wherein said dopant cannot substantially be implanted into said offset regions.

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22. (Twice Amended) A method of manufacturing thin film transistors

comprising the steps of:

D3  
Unit

(a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;

(i) forming a gate insulating film on and across an intermediate region of said substrate, said film covering at least a portion of said semiconductor layers, the gate insulating film having a thickness not larger than 50 nm, and exposing end regions of each of the semiconductor layers;